L Number	Hits	Search Text	DB	Time stamp
1	2354	438/106,108,113,615-617.ccls.	USPAT; US-PGPUB	2003/02/12 16:03
2	135	438/106,108,113,615-617.ccls. and (wafer or substrate or chip) and interposer	USPAT; US-PGPUB	2003/02/12 16:05
3	34	(438/106,108,113,615-617.ccls. and (wafer or substrate or chip) and interposer) and dicing	USPAT; US-PGPUB	2003/02/12 16:05

L Number	Hits	Search Text	DB	Time stamp
1	34	(438/106,108,113,615-617.ccls. and (wafer or substrate or chip) and interposer) and dicing	USPAT; US-PGPUB	2003/02/13 10:44
2	30	((438/106,108,113,615-617.ccls. and (wafer or substrate or chip) and interposer) and dicing) and (electrical or testing)	USPAT; US-PGPUB	2003/02/13 10:25
3	0	(438/106,108,113,615-617.ccls. and (wafer or substrate or chip) and interposer) and dicing	EPO; JPO; DERWENT; IBM_TDB	2003/02/13 10:45
5	4	(wafer or substrate or chip) same interposer and dicing and testing	EPO; JPO; DERWENT; IBM_TDB	2003/02/13 10:45

	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR
1	☐	☒	US 20010044197 A1	20011122	17	WAFER-SCALE ASSEMBY OF CHIP-SIZE PACKAGES	438/612
2	☐	☒	US 6476503 B1	20021105	49	Semiconductor device having columnar electrode and method of manufacturing same	257/780
3	☐	☒	US 6432744 B1	20020813	16	Wafer-scale assembly of chip-size packages	438/108
4	☐	☒	US 6413799 B1	20020702	7	Method of forming a ball-grid array package at a wafer level	438/113
5	☐	☒	US 6372527 B1	20020416	43	Methods of making semiconductor chip assemblies	438/15
6	☐	☒	US 6294407 B1	20010925	23	Microelectronic packages including thin film decal and dielectric adhesive layer having conductive vias therein, and methods of fabricating the same	438/118
7	☐	☒	US 6284563 B1	20010904	25	Method of making compliant microelectronic assemblies	438/106
8	☐	☒	US 5915170 A	19990622	15	Multiple part compliant interface for packaging of a semiconductor chip and method therefor	438/118
9	☐	☒	US 5848467 A	19981215	42	Methods of making semiconductor chip assemblies	29/841
10	☐	☒	US 5346861 A	19940913	20	Semiconductor chip assemblies and methods of making same	438/15

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1	438/617		HEINEN, KATHERINE G. et al.	☒	☐	☐	☐	☐	☐	☐	US 20010044197	☐
2	257/737; 257/773; 257/778; 361/779; 438/615		Imamura, Kazuyuki et al.	☒	☐	☐	☐	☐	☐	☐	US 6476503	☐
3	438/118; 438/612; 438/616		Amador, Gonzalo et al.	☒	☐	☐	☐	☐	☐	☐	US 6432744	☐
4	438/118; 438/458		Lam, Ken M.	☒	☐	☐	☐	☐	☐	☐	US 6413799	☐
5	438/113; 438/125		Khandros, Igor Y. et al.	☒	☐	☐	☐	☐	☐	☐	US 6372527	☐
6	438/108; 438/110		Jacobs, Scott L.	☒	☐	☐	☐	☐	☐	☐	US 6294407	☐
7	438/127		Fjelstad, Joseph	☒	☐	☐	☐	☐	☐	☐	US 6284563	☐
8	438/106		Raab, Kurt et al.	☒	☐	☐	☐	☐	☐	☐	US 5915170	☐
9	29/832; 29/840; 29/842; 438/113		Khandros, Igor Y. et al.	☒	☐	☐	☐	☐	☐	☐	US 5848467	☐
10	29/832; 438/113; 438/125		Khandros, Igor Y. et al.	☒	☐	☐	☐	☐	☐	☐	US 5346861	☐

US-PAT-NO: 6294407

DOCUMENT-IDENTIFIER: US 6294407 B1

TITLE: Microelectronic packages including thin film decal and dielectric adhesive layer having conductive vias therein, and methods of fabricating the same

---------- KWIC ---------

FIG. 10 illustrates yet another embodiment of microelectronic packages according to the present invention. As shown in FIG. 10, microelectronic package 1000 includes an elastomeric **interposer** 1010 between the thin film decal 110 and the first level substrate 102. The elastomeric **interposer** includes an elastomeric stress buffer 1012, a layer of anisotropic conductive adhesive 1014a and 1014b on opposite surfaces of the elastomeric stress buffer 1012 and a vertical thin film 1016 that electrically connects both sides of the **interposer**. The coating of anisotropic adhesive 1014a and 1014b may be used to make electrical contact on both sides of the **interposer** 1010. However, it will be understood that many other techniques may be used to establish this electrical contact. The **interposer** 1010 may be attached first to the first level package 102, to the second level package 120, or both contacts may be made simultaneously. Exceptional stress relief may be obtained.

Accordingly, a PGP die block may be considered a photolithographically fabricated passive IC containing primarily thin film interconnect. Other

electronic structures which support a system may be contained in the decal, such as embedded passives including capacitors, resistors, etc. The PGP is processed on a process substrate well suited for fine line lithography, such as polished silicon wafer, glass, quartz, etc. A process substrate includes at least one die block. A plurality of die blocks may be obtained by **dicing** the process substrate. The thin film layers on this block are then transferred to the surface of a low density interconnect substrate such as a PCB and electrically connected to the thick film substrate by means of conductive and dielectric adhesives, such as silver filled epoxy and silica filled epoxy, interposed between the thin film and the low density substrate. Thus, layers of high density interconnect may be fabricated "en masse" on a lithographically ideal substrate and then transferred to a PCB, rather than trying to build up high density interconnects on a PCB.

US-PAT-NO: 6291270

DOCUMENT-IDENTIFIER: US 6291270 B1

TITLE: Revealing localized cutting line patterns in a semiconductor device

---------- KWIC ---------

A method of production of a semiconductor device having bumps on its surface
and having spaces between the bumps sealed by a resin capable of cutting a
wafer accurately positioned to cutting lines giving a cutting margin on the
wafer in a dicing step of the semiconductor device. On a semiconductor wafer
10 in which circuit patterns of semiconductor chips are formed in a first
region and cutting lines 16 between semiconductor chips are formed extending
across the first region and a second region, bumps are formed so as to be
connected to the circuit patterns of the semiconductor chips, a resin coating
15 is formed on a bump forming surface of the semiconductor wafer to a
predetermined thickness in the first region while sealing the spaces between
the bumps and to a thickness enabling confirmation of positions of parts of the
cutting lines in regions 16a containing at least the parts of the cutting lines
in the second region, and the semiconductor wafer is cut along the cutting
lines using as reference positions the cutting lines confirmed in the regions
containing at least the parts of the cutting lines in the second region.

An explanation will be made next of a semiconductor device of the above CSP
format and a method for mounting it. For example, as shown

in the sectional
view of FIG. 1A, not illustrated electrode pads and a base board (**interposer**)
11 of a semiconductor chip 10a are mechanically and electrically connected by
solder or other bumps 12. Further, the space between the semiconductor chip
10a and the base board 11 is filled and sealed by a sealing resin 13 for
protecting the connections by the bumps 12. Further, the surface of the base
board 11 opposite to the surface connected to the semiconductor chip 10a is
formed with solder or other bumps 14 for connection to a mother board. The
bumps 14 are connected to the bumps 12 connecting the electrode pads of the
semiconductor chip 10a and the base board 11 via not shown through holes or
other interconnections formed in the base board 11. Due to these, a
semiconductor device 100 of a CSP format is formed.

The above semiconductor device 100 has the base board (**interposer**) 11 acting as
a buffer between the semiconductor chip 10a and the mother board 2, but
research and development for a CSP of a format applying packaging at a wafer
level without using the above base board (**interposer**) are now being actively
carried out for a further reduction of size, lowering of cost, and improvement
of processing speed of electronic circuits.

An explanation will be made next of a semiconductor device of a CSP format not
using the above base board (**interposer**) and the method for mounting it. For
example, as shown in the sectional view of FIG. 2A, solder or other bumps 12
are formed connected to not illustrated electrode pads of the semiconductor
device 10a. The surface of the semiconductor chip 10a in the space between the
bumps 12 is sealed by a resin coating 15. By this, a semiconductor device 1 of

a CSP format is formed. On the other hand, the mother board 2 for mounting the semiconductor device 1 has the lands (electrodes) 21 and a not illustrated printed circuit on the top surface of board 20 made of for example a glass epoxy-based material in the same way as the above description. The above semiconductor device 1 is mounted on the mother board 2 by facing the bump forming surface of the semiconductor device 1 to the land forming surface of the mother board 2 while aligning the corresponding lands 21 and bumps 12, and, as shown in FIG. 2B, by using a method of making the bumps 12 reflow etc., the semiconductor device 1 and the lands 21 of the mother board 2 are connected mechanically and electrically via the bumps 12.

Next, as shown in FIG. 4C, the semiconductor wafer 10 is cut (**dicing** step) along cutting lines comprised of regions between the circuit patterns of the semiconductor chips formed on the semiconductor wafer 10 and giving cutting margins of the semiconductor wafer 10 so as to divide it into semiconductor devices 1 of the CSP format each having cut semiconductor chips 10a and unnecessary parts 3 comprised of the outer periphery of the semiconductor wafer 10 not having complete circuit patterns.

The semiconductor device 1 produced by the above method of production can be mounted on the mother board as it is after **dicing** the semiconductor wafer 10, and enables a reduction of costs and a shortening of a delivery compared with conventional semiconductor devices using a base board (**interposer**).

The present invention was made in consideration with the above problem. The present invention has as its object to provide a method of production of a

semiconductor device of a package format comprised of a semiconductor chip having bumps on its surface with spaces between bumps on the bump forming surface sealed by a resin, wherein it is possible to cut a semiconductor wafer accurately aligned with cutting lines forming cutting margins on the semiconductor **wafer in the dicing** step for producing the semiconductor device.

Next, as shown in FIG. 8C, the semiconductor wafer 10 is cut (**dicing** step) along the cutting lines comprised of the regions between circuit patterns of the semiconductor chips formed on the semiconductor wafer 10 in the first region A and the second region B and giving cutting margins of the semiconductor wafer 10 to divide it into semiconductor devices 1 of the CSP format each having cut semiconductor chips 10a and an unnecessary part 3 comprised of the outer periphery of the semiconductor wafer 10 which does not have complete circuit patterns. Here, in cutting the semiconductor wafer 10 along the cutting lines, the positions of the cutting lines are visually confirmed from the underlying patterns seen through the thin resin coating 15 or an image of the semiconductor wafer 10 is taken by a CCD camera or the like and the obtained image is processed on a computer to confirm the positions of the cutting lines and then the semiconductor wafer 10 is cut along the cutting lines using as reference positions the confirmed cutting lines.

Next, as shown in FIG. 12C, the semiconductor wafer 10 is cut (**dicing** step) along the cutting lines comprised of the regions between circuit patterns of the semiconductor chips formed on the semiconductor wafer 10 in the first region A and the second region B and giving cutting margins

of the
semiconductor wafer 10 to divide it into semiconductor devices 1 of the CSP
format each having cut semiconductor chips 1a and an unnecessary part 3
comprised of the outer periphery of the semiconductor wafer 10 which does not
have complete circuit patterns. Here, in cutting the semiconductor wafer 10
along the cutting lines, the positions of the cutting lines are visually
confirmed from the underlying patterns seen through the thin resin coating 15
or an image of the semiconductor wafer 10 is taken by a CCD camera or the like
and the obtained image is processed on a computer to confirm the positions of
the cutting lines and then the semiconductor wafer 10 is cut along the cutting
lines using as reference positions the confirmed cutting lines.

US-PAT-NO: 6413799

DOCUMENT-IDENTIFIER: US 6413799 B1

TITLE: Method of forming a ball-grid array package at a wafer level

---------- KWIC ---------

A method of forming an integrated circuit at the wafer level. The integrated circuit package occupies a minimum amount of space on an end-use printed circuit board. A pre-fabricated interposer substrate, made of metal circuitry and a dielectric base, has a plurality of metallized openings which are aligned with metallized wirebond pads on the top surface of a silicon wafer. Solder, or conductive adhesive, is deposited through the metallized openings to form the **electrical** connection between the circuitry on the interposer layer and the circuitry on the wafer. Solder balls are then placed on the metal pad openings on the interposer substrate and are reflowed to form a wafer-level BGA structure. The wafer-level BGA structure is then cut into individual BGA chip packages.

The footprint of an integrated circuit package on a circuit board is the area of the board occupied by the package. It is generally desired to minimize the footprint and to place packages close together. In recent years, the ball-grid array (BGA) package has emerged as one of the more popular package types because it provides high density, minimum footprint, and shorter **electrical** paths, which means that it has better performance than previous types of

semiconductor packages.

In the prior art, as described above, it is common to fabricate a package for each individual die. Others have realized that it would be advantageous to be able to form the IC package at the wafer level, that is, after the individual chips have been formed on the wafer but before the wafer has been diced into individual chips. This allows for easier mass production of chip packages and for several chip packages, arranged in a matrix format on the wafer, to be manufactured and tested all at one time. This can reduce time and cost in the process of packaging and **testing** IC chips.

Some examples of packaging methods in the prior art that are conducted at the wafer level include: U.S. Pat. No. 5,604,160 to Warfield, which discloses using a cap wafer to package semiconductor devices on a device wafer; U.S. Pat. No. 5,798,557 to Salatino et al., which describes a wafer level hermetically packaged integrated circuit having a protective cover wafer bonded to a semiconductor device substrate wafer; and U.S. Pat. No. 5,851,845 to Wood et al., which discloses a method of forming a semiconductor package by providing a wafer containing a plurality of dice, thinning a backside of the wafer by polishing or etching, attaching the thinned **wafer to a substrate, and then dicing the wafer**.

It is a further object of the invention to provide a method of forming such an IC package at the wafer level in order to take advantage of the greater efficiency in mass production and the ability to conduct parallel **testing** of the IC packages.

The above objects have been achieved in a method of forming

an integrated
circuit package on the wafer level using a flip chip design with a single
wafer. The integrated circuit package is formed by first providing a product
silicon wafer having a plurality of microelectric circuits fabricated thereon
and having a plurality of standard aluminum bonding pads exposed. The aluminum
bonding pads are re-metallized to be solderable. Then, a layer of adhesive is
deposited onto the wafer surface, the bonding pads remaining exposed. A
pre-fabricated interposer substrate, having metallized openings, is aligned to
the wafer and then the assembly is cured. Solder, or conductive adhesive, is
then deposited through the openings in the substrate and the assembly is
reflowed, or cured, to form the **electrical** connection between the circuitry on
the substrate and the bonding pads on the silicon wafer. Solder balls are then
placed on the metal pads on the substrate and are then reflowed forming a BGA
structure. The wafer is then diced and the individual BGA packages are formed.
The BGA package is flipped for mounting on a circuit board.

The integrated circuit package of the present invention is smaller than BGA
packages of the prior art in that the additional space usually required because
of the use of wirebonding leads is not necessary. The whole wafer can be
packaged all at one time which is more efficient than packaging each die
individually and allows for parallel **testing** of the packaged dice while still
in wafer form.

With reference to FIG. 6, a layer of solder paste 40 is deposited through the
openings 36 of the interposer substrate 30. This can be carried out by a
screen or stencil printing process in the same manner as described above with

reference to the depositing of the elastomer layer 27. The interposer substrate base 32 layer is screened off and the solder paste 40 is deposited into the openings 36 by an air-operated squeegee so that the solder paste 40 is deposited on the wafer all at one time. The wafer 21 is then solder reflowed to form a plurality of **electrical** connections between the bonding pads 23 on the wafer 21 and the copper metal circuitry 34 in the interposer substrate layer 30. The solder paste can also be deposited through the openings of the interposer substrate by the use of automatic dispensing equipment or by solder preform placement. Alternatively, a conductive adhesive may be used, in lieu of the solder paste, to electrically connect the bonding pads 23 and the metal circuitry 34. The adhesive is deposited in the openings 36 and then is cured to form the **electrical** connections. Optionally, an epoxy material can be used to protect the solder connections. Application of the epoxy material would also be by the screen or stencil printing process described above and the protective coating would then be cured.

At this point, **electrical testing** may be conducted on the wafer assembly 39 since the wafer assembly 39 contains finished dice arranged in a matrix format. This allows for parallel **testing,** which can be conducted at the wafer level and can provide savings in **testing** time and cost. Then the wafer assembly 39 is diced, or singulated, to form individual chip-size BGA packages 70, 72. A common technique for the singulation is to use a wafer saw with diamond or resinoid saw blades. With reference to FIG. 8, the finished BGA package 70 can then be mounted on the end-use printed circuit board in the same manner as prior art BGA packages. The BGA package 70 of the present

invention has the
same footprint as the individual silicon die, as no extra space is needed to
accommodate wirebond leads or larger substrate bases. In this way, the
integrated circuit package of the present invention provides the advantages of
a smaller package size and the convenience of packaging at the wafer level.

forming an **electrical** connection between the plurality of metallized openings
and the plurality of bonding pads,

lastly **dicing the wafer** assembly into a plurality of individual integrated
circuit chip packages.

8. The method of claim 1 wherein the step of forming an **electrical** connection
between the plurality of metallized openings and the plurality of bonding pads
includes:

reflowing the layer of solder to form an **electrical** connection.

9. The method of claim 1 wherein the step of forming an **electrical** connection
between the plurality of metallized openings and the plurality of bonding pads
includes:

curing the layer of conductive adhesive to form an **electrical** connection.

forming an **electrical** connection between the plurality of metallized openings
and the plurality of bonding pads,

lastly **dicing the wafer** assembly into a plurality of individual integrated
circuit chip packages.

11. The method of claim 10 wherein the step of forming an **electrical**
connection between the plurality of metallized openings and

the plurality of
bonding pads includes:

reflowing the layer of solder to form an **electrical** connection.

12. The method of claim 10 wherein the step of forming an **electrical** connection between the plurality of metallized openings and the plurality of
bonding pads includes:

curing the layer of conductive adhesive to form an **electrical** connection.